Design of Ram Memory in the Era of VLSI for Low Power Dissipation

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ABSTRACT:

This project describes the design of 2 to 4 line decoders using transmission gate logic, pass transistor logic, and a static CMOS logic. All the logics contain full voltage swing capability and less transistor count in their designs compared to their conventional CMOS technology. Finally, a comparative analysis provides that the proposed logic i.e., mixed logic, results a significant improvement in power consumption and area in terms of transistor count. With the motivation of this and by using the proposed 2 to 4 line decoder as base an higher order decoders like 3 to 8 and 4 to 16 decoders are also designed and compared with the conventional CMOS methodology.Further, a 4X4 RAM Memory is designed as an application to illustrate that with this design methodology more number of digital circuits can be designed.

I. INTRODUCTION

Static CMOS circuits are used for the vast majority of logic gates in integrated circuits. They consist of complementary *N* - type metal-oxide-semiconductor (NMOS) pull down and P-type metal-oxide semiconductor (PMOS) pull up networks and present good performance as well as resistance to noise and device variation. Therefore, complementary metal-oxide semiconductor (CMOS) logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes . Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design.

Pass transistor logic (PTL) was mainly developed in the 1990s, when various design styles were introduced, aiming to provide a viable alternative to CMOS logic and improve speed, power, and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual NMOS/PMOS pass transistors or parallel pairs of NMOS and PMOS called transmission gates.

Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g., SRAM). This brief develops a mixed-logic methodology for their implementation, opting for improved performance compared to single-style design, the rest of this brief is organized as follows: Section II provides a brief overview of the examined decoder circuits, implemented with conventional CMOS logic. Section III introduces the new mixed-logic designs. Section IV conducts a comparative simulation study among the proposed

and conventional decoders, with a detailed discussion on the derived results. Section V provides the summary and final conclusions of the work presented.

II. LINE DECODERS

In digital systems, discrete quantities of information are represented by binary codes. An *n*-bit binary code can represent up to 2^n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from *n* input lines to a maximum of 2^nunique output lines or fewer if the *n*-bit coded information has unused combinations. The circuits examined here are *n*-to-*m* line decoders, which generate the $m = 2^n$min-terms of *n* input variables

Table I Truth Table of 2–4 Decoder

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

Table II Truth Table of Inverting 2–4 Decoder

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

III. MIXED LOGIC DESIGN

A. 14-Transistor 2–4 Low-Power Topology

Designing a 2–4 line decoder with either TGL or DVL gates would require a total of 16 transistors (12 for AND/OR gates and 4 for inverters). However, by mixing both AND gate types into the same topology and using proper signal arrangement, it is possible to eliminate one of the two inverters, therefore reducing the total transistor count to 14.

Let us assume that, out of the two inputs, namely, *A* and *B*, we aim to eliminate the *B* inverter from the circuit. The *Do* minterm (*A_B_*) is implemented with a DVL gate, where *A* is used as the propagate signal. The *D*1 minterm (*AB_*) is implemented with a TGL gate, where *B* is used as the propagate signal. The D2 minterm (*A_B*) is implemented with a DVL gate, where *A* is used as the propagate signal.

Finally, The *D*3 minterm (*AB*) is implemented with a TGL gate, where *B* is used as the propagate signal. These particular choices completely avert the use of the complementary *B* signal; therefore, the *B* inverter can be eliminated from the circuit, resulting in a 14-transistor topology (9 nMOS and 5 pMOS). Following a similar procedure with OR gates, a 2–4 inverting line decoder can be implemented with 14 transistors (5 nMOS and 9 pMOS) as well: *I*0 and *I*2 are implemented with TGL (us-ing *B* as the propagate signal), and *I*1 and *I*3 are implemented with DVL (using *A* as the propagate signal). The *B* inverter can once again be elided. Inverter elimination reduces the transistor count, logical effort and overall

switching activity of the circuits, thereby reducing power dissipation. The two new topologies are named "2–4LP" and "2–4LPI," where "LP" stands for "low power" and "I" for "inverting." Their schematics are shown in Fig. 1(a) and (b), respectively.

B. 15-Transistor 2–4 High-Performance Topology

The low-power topologies presented above have a drawback regarding worst case delay, which comes from the use of complementary A as the propagate signal in the case of *D*0 and *I*3. However, *D*0 and *I*3 can be efficiently implemented using static CMOS gates, without using complementary signals. Specifically, *D*0 can be implemented with a CMOS NOR gate and *I*3 with a CMOS NAND gate, adding one transistor to each topology. The new 15T designs present a significant improvement in delay while only slightly increasing power dissipation. They are named "2–4HP" (9 nMOS, 6 pMOS) and "2–4HPI" (6 nMOS, 9 pMOS), where "HP" stands for "high performance" and "I" stands for "inverting." The 2–4HP and 2–4HPI schematics are shown in Fig. 2(a) and (b), respectively.

C. Integration in 4–16 Line Decoders

PTL can realize logic functions with fewer transistors and smaller logical effort than CMOS. However, cascading PTL circuits may cause degradation in performance due to the lack of driving capability. Therefore, a mixed topology approach, i.e., alternating PTL and CMOS logic, can potentially deliver optimum results.

We implemented four 4–16 decoders by using the four new 2–4 as predecoders in conjunction with CMOS NOR/NAND gates to produce the decoded outputs. The new topologies derived from this combination are the following: 4–16LP [Fig. 3(a)], which combines two 2–4LPI predecoders with a NOR-based postdecoder; 4–16HP [Fig. 3(b)], which combines two 2–4HPI predecoders with a NOR-based postdecoder; 4–16LPI [Fig. 3(c)], which combines two 2– 4LP pre decoders with a NAND-based post decoder; and, finally, 4–16HPI [Fig. 3(d)],which combines two 2–4HP predecoders with a NAND-based postdecoder. The "LP" topologies have a total of 92 transistors, while the "HP" ones have 94, as opposed to 104 with pure CMOS.

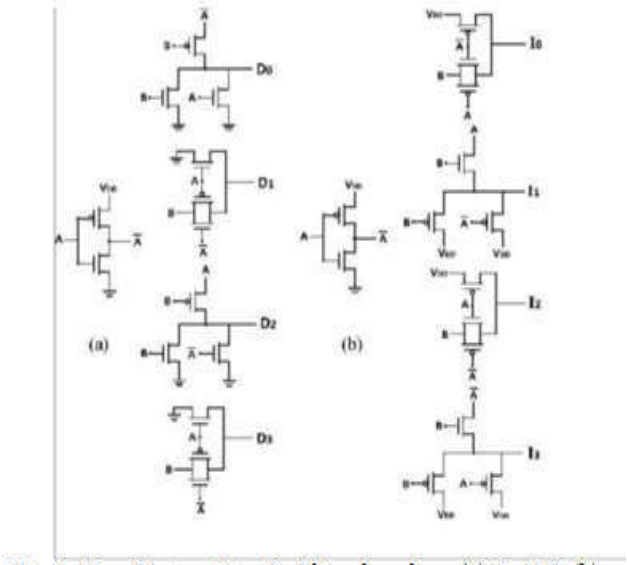


Fig. 1. New 14-transistor 2–4 line decoders. (a) 2–4LP. (b) 24LPI

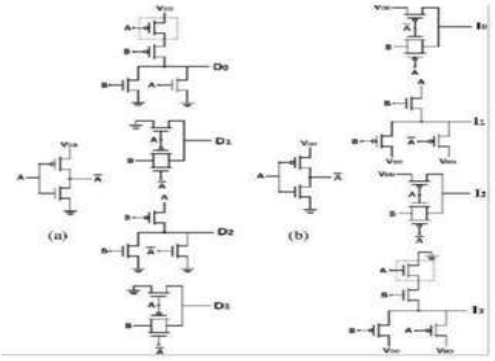


Fig. 2. New 15-transistor 2–4 line decoders. (a) 2–4HP. (b) 2–4HPI

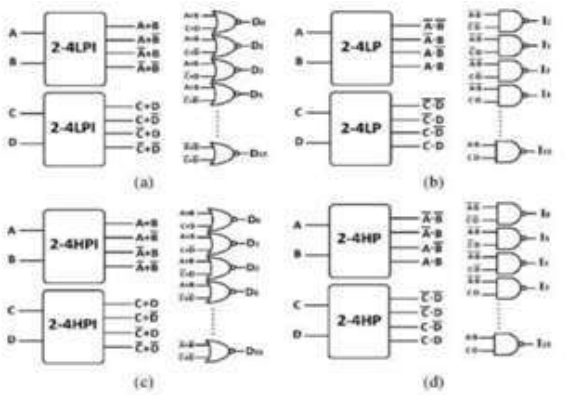


Fig. 3. New 4–16 line decoders. (a) 4–16LP. (b) 4–16LPI. (c) 4–16HP. (d) 4–16HPI

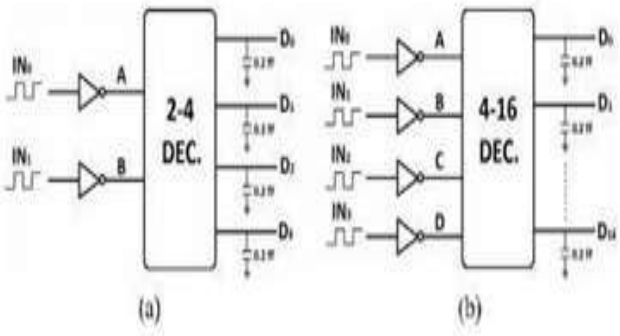
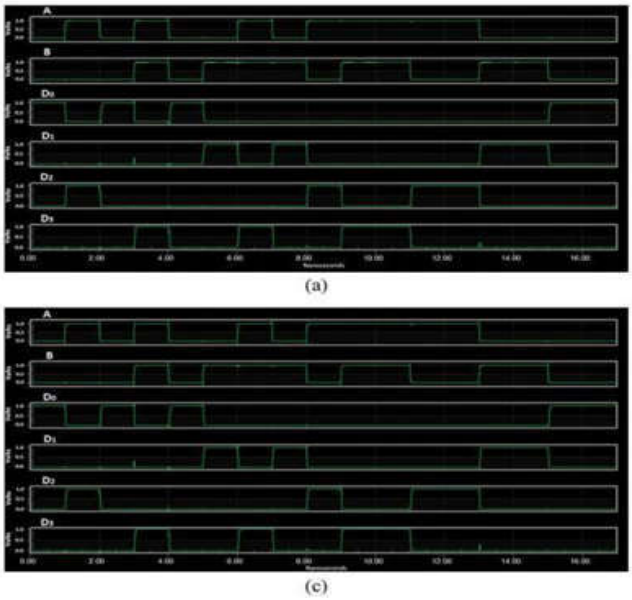


Fig. 4. Simulation setup regarding input/output loading conditions. (a) 2–4 de-coders. (b) 4–16 decoders

IV. SIMULATION RESULTS



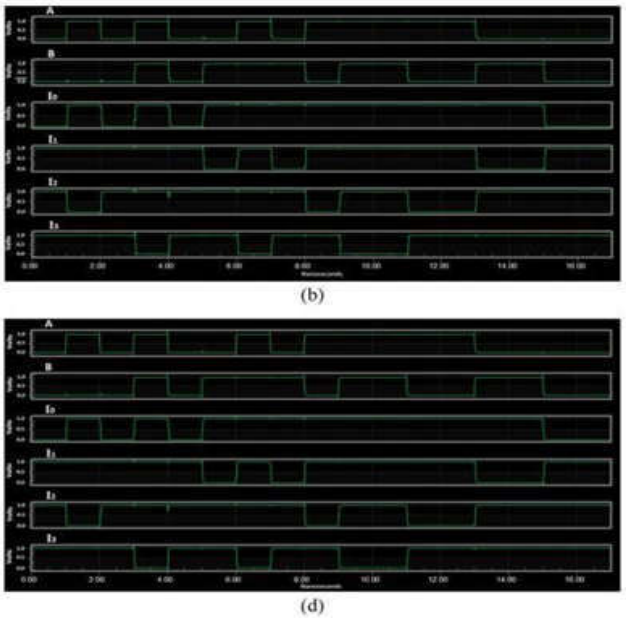


Fig. 5. I/O waveforms of the proposed 2–4 decoders for all input transitions. (a) 2–4LP. (b) 2–4LPI. (c) 2–4HP. (d) 2–4HPI

In this section, we perform a variety of BSIM4-based spice simulations on the schematic level, in order to compare the proposed mixed-logic decoders with the conventional CMOS. The circuits are implemented using a 32 nm predictive technology model for low-power applications (PTM LP), incorporating high-*k*/metal gate and stress effect [11]. For fair and unbiased comparison we use unit-size transistors exclusively ($L_n = L_p = 32$ nm, $W_n = W_p = 64$ nm) for all decoders.

A. Result Discussion

The simulation results regarding power, PDP and delay are analyzed by comparatively. Each of the proposed de-signs will be compared to its conventional counterpart. Specifically, 2–4LP and 2–4HP are compared to 20T, 2–4LPI and 2–4HPI are compared to inverting 20T, 4–16LP and transitions. (a) 2–4LP. (b) 2–4LPI. (c) 2–4HP. (d) 2–4HPI 4–16HP are compared to 104T and finally,

4– 16LPI and 4–16HPI are compared to inverting 104T.

According to the obtained results, 2–4LP presents 9.3% less power dissipation than CMOS 20T, while introducing a cost of 26.7% higher delay and 15.7% higher PDP. On the other hand, 2–4HP outperforms CMOS 20T in all aspects, reducing power, delay, and PDP by 8.2%, 4.3%, and 15.7%, respectively. Both of our inverting designs, 2–4LPI and 2–4HPI, outperform CMOS 20T inverting in all aspects as well. Specifically, 2–4LPI reduces power, delay, and PDP by 13.3%, 11%, and 25%.

V. RAM Design

The binary cell has three inputs and one output. The select input enables the cell for reading or writing and the reda/write input determines the cell operation when it is selected. A 1 in the read/write input provides the read operation by forming a path from the flip-flop to the output terminal. A 0 in the read/write input provides the write operation by forming a path from the input terminal to the flip-flop figure 6 illustrates the internal schematic of basic cell.

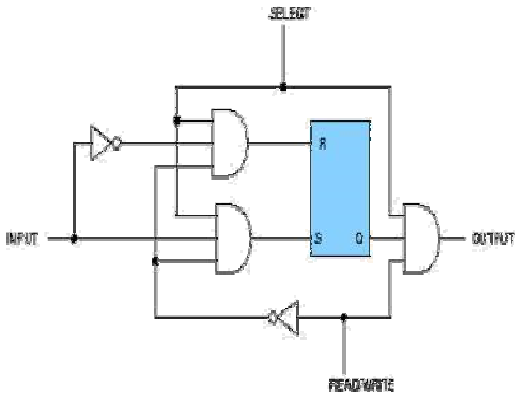


Fig.6: Internal Schematic of Basic Cell

4X4 RAM Design

The logical construction of a 4X4 RAM is shown in figure 8. It consists of 4 words of 4 bits each and has a total of 16 binary cells. Each block labeled as BC, which represents the basic cell with its 3 inputs and 1 output. The block diagram of a basic cell is shown in the figure 7.

A memory with 4 words needs two address lines. First, the decoder is enable by the memory enable pin and the two address inputs selects the required word among the four words in the design of 2 to 4 decoder.

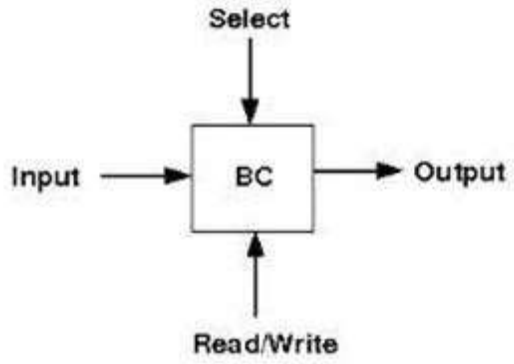


Fig. 7: Basic cell block

If the enable pin i.e., control pin of memory is 0 then all of the word lines are 0. When the control pin of memory is 1 then one of the word line is selected depending on the input address lines combination. Read or Write pin determines the operation of the memory after the selection of word line; the logic diagram is shown in the figure 8.

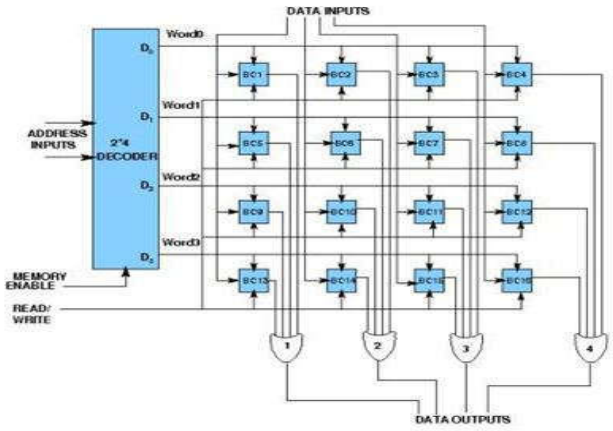


Fig. 8: 4X4 RAM memory using 2 to 4 decoder

Table III: Comparison of 4X4 RAM memory

	Conventional logic	Proposed logic
Transistors count(T)	828	814
Power	184µw	107µw

CONCLUSION:

In the present scenario, there is a rapid development in the design of IC technology. In that, low power is a challenging one, due to all electronic devices are trying to design with low power applications. So, an attempt is made to design a low power decoders using different logics such as DPL, DVL, TGL and a mixed logic. From the results obtained it is clear that mixed logic design provides less power in the design of 2 to 4 decoder.

By considering this low power decoder as a base the higher order decoders, 3 to 8 and 4 to 16 are also designed. From the motivation of this, a 4X4 RAM is also implemented and compared with the conventional one, and from the comparison table, 4X4 RAM using proposed decoder consumes less power. Finally, it is concluded that using mixed logic a low power decoder and a RAM is designed.

In future, even more combinational circuits like encoder, multiplexer, de-multiplexer, etc., can be designed using mixed logic.

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