GRID CONNECTION OF SUB SEA POWER CABLE EMULATROR

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Abstract—*This work proposes a new transmission line emulation system designed to test the performance of subsea power electronics systems within a power hardware-in-the-loop (P-HIL) framework. The emulator is composed of cascaded lumped parameter line equivalent sections, where all resistors of the transmission line electric model are replaced by regenerative power converters. These are employed to emulate a given behavior of relatively wide frequency band loss free resistors. Thus, most of the ohmic losses in a given test setup are avoided and the energy can be injected back to the grid. Furthermore, this emulator allows to reproduce the most significant harmonics including some of the resonance effects in the system under test. Many challenges and relevant topics of power electronics are discussed. These include high performance converters, power ripple across the dc-link of the ac-dc rectifiers, state of the art gallium nitride (eGaN) power devices, and the proposed control structure. Index Terms—Power Hardware-in-the-loop (P-HIL), Transmission Line Emulator, Subsea Variable Speed Drives (VSD), Extreme Performance Single Phase Rectifiers.*

Keywords: Transmission Line Emulator, Subsea variable Speed drives, P-HIl

1. INTRODUCTION

In offshore power systems, remote plants and connections through long submarine power cables, also known as submarine power umbilical's, generate significant voltage drops and losses. Due to resonances that naturally occur in setups with power umbilical's, it is important to forecast the effects of the harmonic content generated by the interactions between power converters, electric motors, and other equipment in the systems. Examples were reported in some applications, such as variable speed subsea motor drives with long step out cables [1] and offshore wind farms [2], [3], where the effects of resonances and delays caused by the reflection of electromagnetic waves influence the dynamic performance of a given system. Furthermore, the relatively high shunt capacitance values of subsea cables lead to reactive power distributions that can be very different from typical onshore industrial installations. Thus, the emulation of such effects in experimental setups presents ever increased importance.

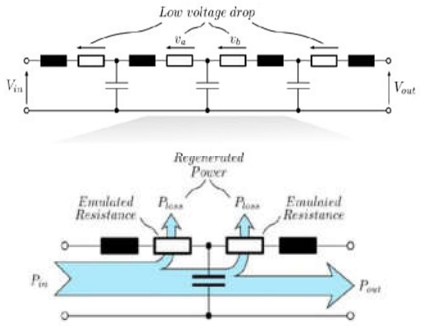

Fig. 1. Hybrid power cable emulator concept and losses diagram in a T-equivalent section. The concept is to implement the resistive voltage drops through high efficiency power converters.

In addition, such experimental setups could benefit from the use of power

converters to improve energy efficiency and to implement more controllable and flexible emulation functions. In order to emulate the transmission line effects, some power hardware-in-loop (P-HIL) [4] or hardware testbed (HTB) [5] technologies were recently reported to operate as power grid cable emulators [5], [6]. However, these approaches are solely focused on the fundamental frequency electrical behavior, while ignoring electric phenomena in a wider frequency spectrum [5].Furthermore, conventional transmission line emulators are typically built based on back to-back voltage source converters (BTB-VSCs) that inevitably lead to low switching frequency when operating within high power medium voltage test setups due to well-known power semiconductor switching speed limitations. On the other hand, a good option to create the frequency dependence including resonances of the real cable impedance consists in the use of classic π- or T-equivalent lumped parameter cable models with cascaded sections. The number of series cascaded sections required ideally depends on the higher observable frequency effects that are demanded for the hardware model to reproduce. The implementation of a high voltage passive power cable emulator was described in [1], where ten cascaded π sections were chosen to replace, in a real power scale, the umbilical cable that was rated for currents up to 300 A and 50 km of length. This emulator was fully based on passive components. However, in many applications to emulate a long step-out cable, a considerable amount of energy is lost in such entirely passive emulation systems. In this context, this work proposes an innovative emulator based on a new concept, as shown in Fig. 1, which consists of a series connected hybrid (passive active) lumped-parameter cable model. It is seen that the reactive components, i.e., inductors and capacitors, are passives ones, while the passive resistances are implemented through active power converters.

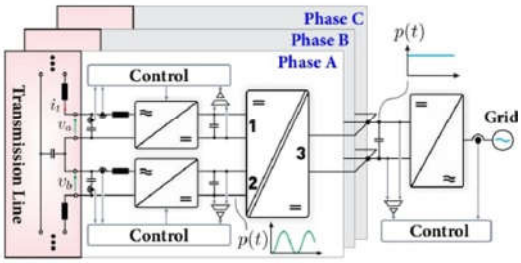

Fig. 2. Power conversion structure of the hybrid power cable emulator including the main control loops and the ideal switching frequency averaged power flows (p(t)). The transmission line section inductances and capacitances are implemented through discrete passive elements, while the resistance behaviour is emulated via the power converters.

Unlike to the BTB-VSC emulator, which would be interfacing the source and load, handling the high voltages Vin and Vout (cf. Fig. 1), in the proposed emulator, each emulated resistance operates with the significantly lower voltages va and vb. This approach enables an advantageous voltage distribution between the elements of the model where high performance low-voltage converters can be used to emulate wide-band resistances. Thus, the emulator allow reproduce significant higher frequency harmonics as with a passive emulator, but in a more flexible and energy efficient focused manner. This paper is organized as follows. **Section II** describes the power conversion structure and the operating principles of the proposed emulator. The main control strategies are proposed in **section III.** Simulation results exemplarily performed by modeling a subsea variable speed drive (VSD) system are presented in **section IV.** Finally, **section V** discusses the conclusions and

future perspectives on the proposed emulation system.

2. POWER CONVERSION ARCHITECTURE

The basic structure of the proposed hybrid emulator is shown in Fig. 2. To design the passive elements of the hybrid emulator, many concepts addressed in [7] can be useful, in special the use of air-core inductors to eliminate the occurrence of magnetic saturation, capacitor technologies and other high voltage issues. In addition, the active portion of the emulator is composed of three power conversion stages. These are implemented through power converters, namely: two rectifiers per phase, one isolated dc-dc converter per phase and a single three-phase inverter. Each stage has the features described in the following.

A. emulation single-phase rectifiers

The main function of this stage is to establish a voltage drop in phase with the current imposed by the system under test along the transmission line, ideally emulating the behavior of a resistance. Considering the target application, the rectifier can be designed with an input voltage range within 40 V. This allows the use of state-of-the-art GaN power semiconductors

in any rectifier topology. However, high currents will flow through the converter and to ensure a wide frequency-band response, the rectifier should present a reduced input filter and be able to achieve low power semiconductor stress levels. A bidirectional rectifier is highly recommended to avoid any unwanted distortion at the input current zero crossings. Several possibilities and concepts for high efficiency rectifiers are found in the literature [8]–[10]. Three-level rectifiers are typically more efficient at high switching frequencies than other 2-level structures. They feature reduced blocking voltages and lower overall filter volume. The differential connection between T-Type legs, as in Fig. 3(a), for instance, produce five levels at the voltage vab, as shown in Fig. 3(b). On the other hand, interleaving these structures as in Fig. 3(c) leads to a 9-level voltage vab, such as depicted in Fig. 3(d). It is an efficient way to reduce current stresses at the semiconductor devices while ensuring filter reduction without the need to increase the switching frequency. The reduction of current levels in the power semiconductors is important since the typical subsea test setup would feature high current levels. A pair of highly coupled inductors ($k \approx 1$) enables low volume of magnetic components, following the concepts discussed in [8], [11], [12]. Moreover, due to required wide frequency response, low voltage enhancement-mode Gallium Nitride eGaN are appropriate. Thus, to fulfill the aforementioned features, a bidirectional version of the interleaved 9-level rectifier (cf. Fig. 3(b)) with low voltage eGaN devices is considered a suitable solution to operate as a wide-band Loss Free Resistor in the proposed emulator. Another important design issue is that single phase ac-dc converters naturally present a dc-link power ripple at twice the ac-side fundamental frequency, which typically demands large dc-link capacitors to limit the voltage ripple at the dclink. In applications such as testing of variable-speed drives (VSD), for instance, this fluctuation will vary according to the speed of the machine, since the machine speed is a function of the transmitted power signal frequency. The proposal here is to allow the propagation of all power fluctuations through the dcdc converter to the common

inverter side dc-bus to overcome this challenge. Thus, the instantaneous low frequency power contributions of the three phases of the emulator ideally add up to a near constant value, as was recently analyzed for solid state transformer (SST) applications [13].

B. Isolated dc-dc converter

This stage enables the required high voltage galvanic isolation between the floating input of the rectifier and the regenerative inverter. Its main function is to operate as a dc transformer, where the dc-link voltage of the rectifiers is set by the regenerative inverter and transformed to feed the rectifiers. The main converter candidates are the dual active bridge (DAB) and the dc-dc resonant converters. The application of both structures was discussed in [13],where it was pointed out that the series resonant converter operated in the half-cycle discontinuous-conduction-mode (SRC-HC-DCM) presents significant advantages for dc transformers in single-phase applications due to its high efficiency and simple control requirements. This is achieved since it ideally operates at constant frequency in an open loop manner.

A three-port version of the SRC is a good option to further compact the power conversion structure as discussed in [14]. In addition, the rectifier dc-link typically requires a low voltage level near to the emulated input voltage. Thus, to ensure the power transfer to the inverter side, a relatively high turns ratio is required. Due to the high current level at the low voltage-side, full-bridge legs can be used, while in the inverter side, three level legs [15] can be an option to reduce voltage stresses. The suggested solution to implement the isolated dc-dc converter stage is presented in Fig. 4(a). Fig. 4(b) shows the relevant resonant

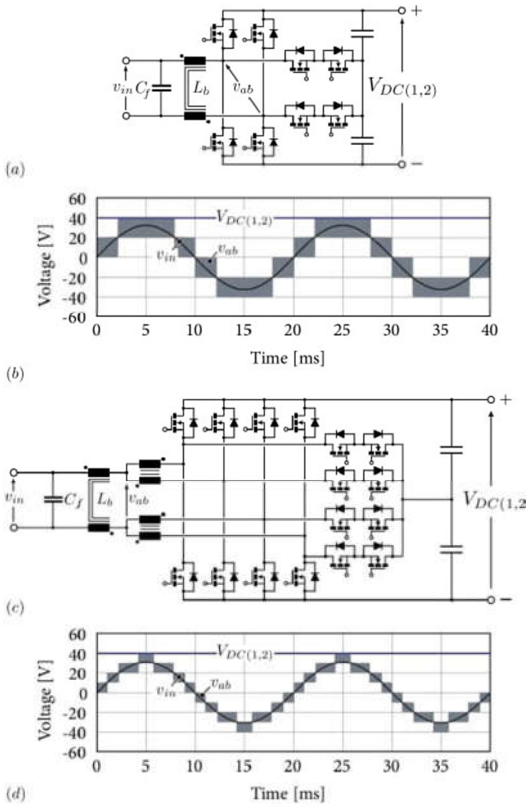

Fig. 3. Candidate high efficiency multilevel single-phase rectifiers: (a) a differential T-Type converter with the main waveforms seen in (b); (c) an interleaved differential T-Type converter using highly coupled inductors (interphase transformers) that features the waveforms depicted in (d).

converter waveforms. The resonant period Tr and the magnetizing current image can be adjusted during the converter design in order to achieve load-independent soft switching ZVS for the switches at ports1 and 2 in normal steady state operation. It is an important feature since the MOSFET non-linear parasitic capacitance (Coss) is discharged in the conductive channel during the turn on transition. The magnetizing current helps to extract the charge of the switch capacitance before the turn on, while Tr defines the zero load current interval. These parameters increase

both the conduction losses and the passive elements losses [15].

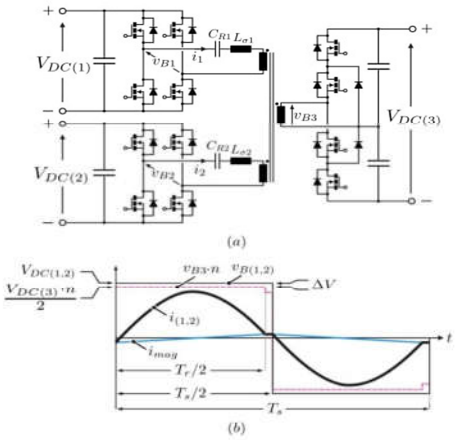

Fig. 4. A three-port discontinuous series resonant dc-dc converter (SRCHC-DCM) (a) topology , which achieves a tight coupling between the two dc voltage bus of the rectifiers with respect to the inverter dc-bus of the proposed cable emulator. Thus, the rectifier-side dc-link voltage is indirectly controlled by a dc-bus control loop at the regeneration inverter stage. And the converter (b) main waveforms. The waveforms are the magnetizing current image, the winding currents i(1,2), the voltages in the windings reflected to the ports 1 and 2 vB(1,2) and nvB3, where n is the transformer turns ratio.

GaN technology offers switches with lower parasitic capacitance than others semiconductors and this significantly contributes to improve the dc-dc converter efficiency. A more detailed review with respect to MOSFET non-linear parasitic capacitance and conditions to ensure soft switching ZVS are addressed in [16]. It is worth noticing that the transfer ratio is close to unity. However, a small voltage difference (ΔV) remains in practice. This is due to load power and the converter losses.

C. Regenerative inverter

The main functions of this stage are: (i) to condition the power generated by the emulated resistances into an ac grid synchronized power and, (ii) to

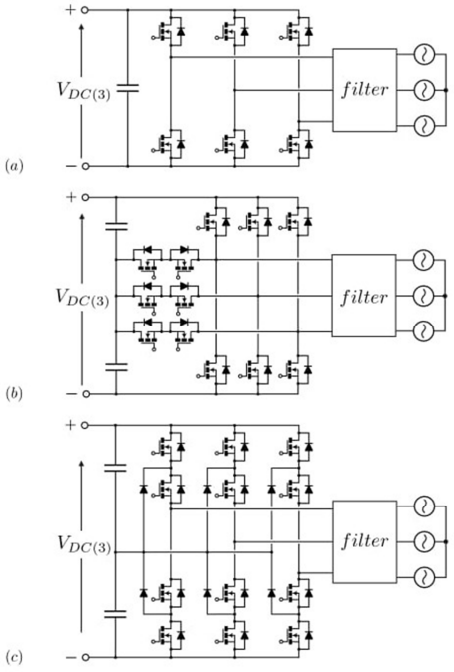

Fig. 5. Three-phase inverter stage topology candidates: (a) conventional two level VSI; (b) three-level T-Type inverter; and, (c) three-level neutral point clamped inverter.

establish a well regulated dc-link voltage for all the other stages. Several types of voltage source converters can be employed depending on the available grid configuration. A three-phase converter generates a very much reduced low frequency power oscillation at its dc-link and, thus, is preferable to fulfill goal (ii). Thus, a natural first option is the 2-level voltage source inverter (VSI) depicted in Fig. 5(a).More advanced options are presented in a comparative and quantitative study of high efficient three phase inverters [17], where it is highlighted that the three level T-type converter (see Fig. 5(b)) typically enables higher efficiency than the other candidates because it provides a third output voltage

level without inserting more passive energy storage components into the system. This leads to a reduced size of the filter inductors compared to the two-level bridge leg variants. However, another comparative evaluation addressed in [18], also shows that the neutral point clamped converter (NPC), depicted in Fig. 5(c), can be more efficient than the T-type depending on the adopted switching frequency, where higher switching frequencies tend to favor the NPC.

3. CONTROL STRUCTURE

The rectifier control is based on averaged current mode control [19]. In addition, the full feedforward strategy proposed in [20] is adopted. This feedforward strategy produces a duty cycle pattern to compensate the input voltage disturbance, as well as computes the inductor voltage contribution, relieving the feedback controller from this task. It also compensates the undesirable boost inductor effect over the input impedance.

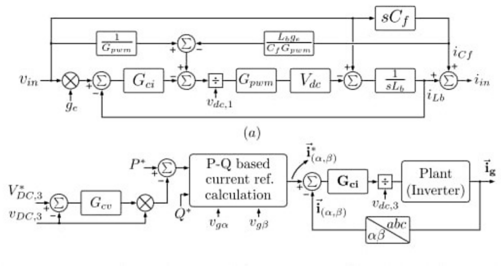

Fig. 6. Proposed control strategy block diagrams: (a) rectifier side control block diagram; and, (b) inverter side pq-theory based αβ control block diagram.

The result is that the converter ideally behaves as a pure resistance and the resulting equivalent input impedance is real and constant over the frequency range of interest. On the other hand, it also contributes to promote active damping to the LC input filter resonances. The proposed modified strategy is depicted on Fig. 6(a) where the derivative of the input voltage proposed in the original feedforward scheme is replaced by a measured capacitor current iCf, which is orthogonal to the input voltage. The conductance ge is a constant value and it refers to a portion of the total cable admittance contained in each section of the transmission line network model. The inverter controls its dc-link voltage VDC(3), while the dc-dc converter provides a tight coupling between the dc-links of its three ports. Consequently, the rectifier dc side VDC(1,2) can be assumed as a constant voltage source. Moreover, a dc feedforward (see Fig. 6(a)) enables a dynamic decoupling to improve the control performance. Therefore, any voltage oscillation at the dc-bus does not affect the rectifier ac side and the input impedance in continuous time can be obtained. It is reduced to

$$Zin = Re/1 + ReCfs \quad (1)$$

where Re = 1 ge is the emulated resistance and Cf is the filter capacitor. The input impedance in (1) presents a first order response. Thus, to avoid a large phase deviation, the pole defined by 1/(ReCf) must be at least half a decade above the maximum frequency where the resistive behavior is desired. In the target subsea VSD application modeling, the spectrum of interest has a maximum frequency of interest of 10 kHz (see Fig. 10). This is typically found by having the knowledge of the main resonance frequencies and the switching frequency of the VSD inverter. In contrast, a 10 kHz control bandwidth leads to the requirement of employing a relatively high switching frequency to operate the emulation rectifiers. The small signal input impedance for the simulated interleaved T-Type rectifier is seen in Fig. 7, where a wide band resistance emulation is achieved. In order to provide a robust

the system stability, a passivity based control design criterion is adopted [21], [22]. It provides

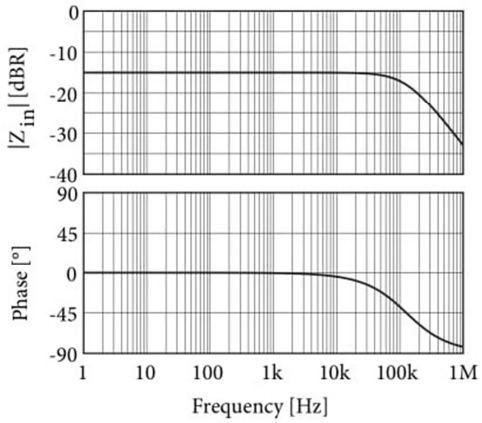

Fig. 7. Input impedance frequency response of the T-Type interleaved converter (see Fig. 3(b)) employing the proposed control strategy. It considers a switching frequency of 250 kHz and continuous time implementation or a digital control with a delay compensation method.

a sufficient stability condition to ensure the stability of the proposed emulator. The stability of each of the rectifiers, which are connected to other converters in the transmission line network can be separately analyzed. This criterion states that if the dynamic analysis of a system component such as a single rectifier is passive, the global stability is not affected by this rectifier, as naturally happens with a passive RLC network for instance. In a simplified way, it means that the real part of the impedance {Zin} should be positive, i.e.,

$$\mathrm{Re}\{Zin\} \geq 0, \quad (2)$$

and, thus, the phase must remain with in

$$\arg\{Zin\} \in \{-\pi/2, \ldots, +\pi/2\} \text{rad} \quad (3)$$

as stated in [22], [23]. Thus, the internal loop phase will not go below $-\pi$ rad. However, this requirement is only applicable to the power converter system since other system components can lead to unpredictable dynamics. Active converters typically can become not passive mainly due to control implementation aspects. In this way, it is well-known that analog controlled converters shows negligible computation and PWM update time. Furthermore, for digitally controlled converters, the control action is calculated in the current sampling period, but the PWM update occurs just in the next sampling instant [24]. This computation delay introduces phase lag in the control loop, which also imposes limitations on the achievable control bandwidth and consequently on the emulated resistance. Due to the discrete nature of the converter control system, the passivity analysis is made up to the Nyquist frequency fs/2 [22], which equivalently corresponds to switching frequency (fsw) for a double update mode PWM. [21], [24]. Power electronics engineers typically adopt current control with a modest crossover frequency, often below fs/10, where

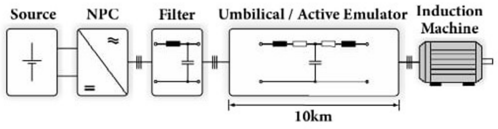

Fig. 8. Employed subsea variable speed drive setup.

the phase deviation due to the delay computation is not significant [25]. However, it is desirable to achieve a high bandwidth without significantly increasing the switching frequency in the emulator system design. A possible way to compensate for these phase lag effects and improve the bandwidth and/or stability of the control loop is to employ some

prediction method, such as addressed in [25], [26], where linear and Smith predictors have shown good performance based on a relatively low computational effort. Additionally, interleaved converters typically use more than one carrier signal in the PWM modulator reducing the update time intervals. On the inverter side, standard voltage oriented control is used[27].The inverter control was implemented in a stationary αβ reference frame (see Fig. 6(b)), where an active power feedforward signal generated by the emulated resistance (P∗) and the dc-bus voltage controller (Gcv) act on the power reference that defines the injected grid current. A reactive power reference (Q∗) can be used if needed.

4. SYSTEM VALIDATION

To validate the emulator design, simulations are performed in a medium voltage variable speed drive model that either employs the proposed emulator or a fully passive version with the same nominal resistances for comparison means. The overall system setup is seen in Fig. 8, where a 3level NPC controls a 11-kV / 1.9-MW induction machine. A power umbilical with a length of 10 km is replaced by the proposed cable emulator, which is composed of a hybrid lumped parameter equivalent model with seven T-equivalent sections. Each section presents up to 5 kW of ohmic losses per phase. The rectifier dc-link voltage is 40 V, while the inverter dc-side voltage is 380 V and the ac-grid line voltage rms value is 220 V. Due to the large number of converters, the emulator stage simulation has been implemented based on state space averaged models.

Fig. 9 shows the waveforms during the machine start-up from standstill to rated speed and torque with a quadratic relation among them. The rectifier draws a voltage drop in phase with the power cable current. Furthermore, the emulator is able to operate in a wide range of variations of the rectifiers input frequency. However, some noise is observed in, both, rectifier and inverter dc-links. It is assumed that all emulator dc-links are pre-charged. Another relevant result is the current injected-back to the grid through the inverter. The results achieved with the proposed active emulator are compared to those with a passive version. The steady-state motor speed condition is used to compare their behaviors in

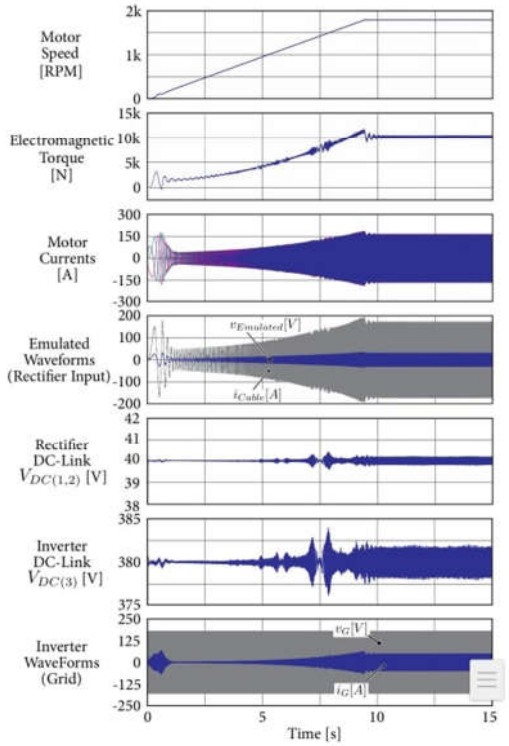

Fig. 9. Main system waveforms during the application of a motor speed ramp like reference.

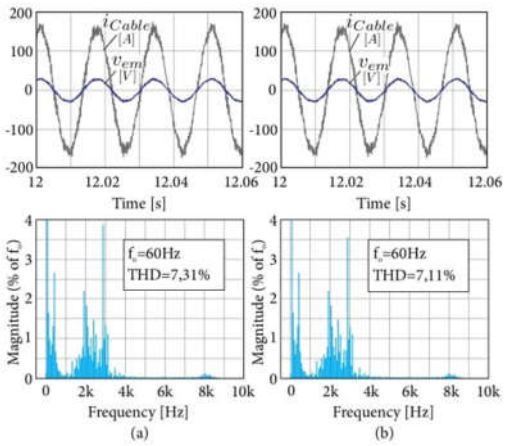

Fig. 10. Comparison of the simulated voltage and current. (a) In a Passive emulator Resistance and (b) in the equivalent proposed active emulator.

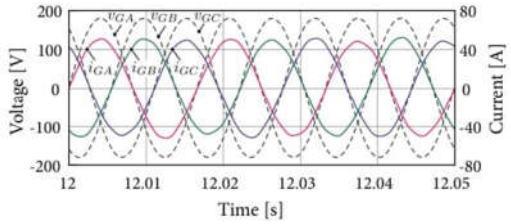

Fig. 11. Detailed waveforms of the regenerative inverter ac-side during steady state. The grid voltages and the grid injected currents are observed. The total power is a sum of the three phases in a single cable hybrid section.

Fig. 10. Both results present similar voltage and current shapes with a very close total harmonic distortion (THD). Multiple resonances can be observed at around 400 Hz, 3 kHz and 8 kHz. These frequencies are, respectively, the NPC output filter and the two main system resonances. Furthermore, the NPC was modulated at a fixed switching frequency of 1 kHz, which justifies major harmonic contents in the 2 kHz range. Synchronous optimum modulation as well as estimator-based control are typically used such setup [1], [28], [29], but a fixed switching frequency PWM modulation suffices to illustrate the emulator functionality and simplifies the performed simulation. Finally, a detailed view of grid voltages and injected currents are presented in Fig. 11, where it is visible that a power of approximately 15 kW return to the grid through of the proposed emulation structure. A single high power inverter could be designed to regenerate the power of all hybrid emulator sections by means of a common dc-bus at a rated voltage of VDC(3).

5. CONCLUSIONS

This work proposed a new power cable emulator concept based on a hybrid (passive active) system based on a cascaded lumped-parameter transmission line model. It emulates the relevant aspects of subsea power cables related to testing variable speed drives. These include resonances and the considerable voltage drop and losses related to long step-out cables. The emulator regenerates a major portion of the otherwise lost energy by using an advanced loss free resistor concept and the significant ohmic losses typically found in the related systems or passive emulators are much reduced. It also allows the validation of control concepts, such as estimator-based control in subsea VSD applications of any real or scaled subsea systems, making it suitable for P-HIL setups, where it provides flexibility and energy efficiency. The main concepts and challenges involved in the design of the proposed emulator were discussed. It is concluded that the use of high-performance converters and current relevant topics of power electronics, such as single-phase dc-link power ripple management, state-of-the-art low voltage

GaN power devices, among others can be advantageously applied. A prototype is currently being developed to a scaled version of a VSD application as the one presented in the validation section.

REFERENCES

[1] B. Monsen, K. S. Rongve, T. Lgreid, and C.Gutscher, "Asgard subsea gas compression - technology qualification testing with high-speed vsd and very long step-out cable," IEEE Transactions on Industry Applications, vol. 50, no. 2, pp. 1552–1561, March 2014.

[2] S. Zhang, S. Jiang, X. Lu, B. Ge, and F. Z. Peng, "Resonance issues and damping techniques for grid-connected inverters with long transmission cable," IEEE Transactions on Power Electronics, vol. 29, no. 1, pp. 110–120, Jan 2014.

[3] P. Bresesti, W. L. Kling, R. L. Hendriks, and R. Vailati, "Hvdc connection of offshore wind farms to the transmission system," IEEE Transactions on Energy Conversion, vol. 22, no. 1, pp. 37–43, March 2007.

[4] M. O. O. Faruque and V. Dinavahi, "Hardware-in-the-loop simulation of power electronic systems using adaptive discretization," IEEE Transactions on Industrial Electronics, vol. 57, no. 4, pp. 1146–1158, April 2010.

[5] B. Liu, S. Zheng, Y. Ma, F. Wang, and L. M. Tolbert, "Control and implementation of converter based ac transmission line emulation," in 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), March 2015, pp. 1807–1814.

[6] S. Zhang, B. Liu, S. Zheng, Y. Ma, F. Wang, and L. M. Tolbert, "Development of a converter-based transmission line emulator with three-phase short-circuit fault emulation capability," IEEE Transactions on Power Electronics, pp. 1–1, 2018.

[7] G. Scheuer, B. Monsen, K. Rongve, T. O. Ronhovd, T. E. Moen, E. Virtanen, and S. Ashmore, "Subsea compact gas compression with high-speed vsds and very long step-out cables," in 2009 Conference Record PCIC Europe, May 2009, pp. 163–173.

[8] M. S. Ortmann, S. A. Mussa, and M. L. Heldwein, "Generalized analysis of a multistate switching cells-based single-phase multilevel pfc rectifier," IEEE Transactions on Power Electronics, vol. 27, no. 1, pp. 46–56, Jan 2012.

[9] Q. Wang, B. Wen, R. Burgos, D. Boroyevich, and A. White, "Efficiency evaluation of two-level and three-level bridgeless pfc boost rectifiers," in 2014 IEEE Applied Power Electronics Conference and Exposition APEC 2014, March 2014, pp. 1909–1915.

[10] A. D. B. Lange, T. B. Soeiro, M. S. Ortmann, and M. L. Heldwein, "Three-level single-phase bridgeless pfc rectifiers," IEEE Transactions on Power Electronics, vol. 30, no. 6, pp. 2935–2949, June 2015.

[11] M. Hirakawa, Y. Watanabe, M. Nagano, K. Andoh, S. Nakatomi, S. Hashino, and T. Shimizu, "High power dc/dc converter using extreme close-coupled inductors aimed for electric vehicles," in The 2010 International Power Electronics Conference - ECCE ASIA -, June 2010, pp. 2941–2948.

[12] D. O. Boillat and J. W. Kolar, "Modeling and experimental analysis of a coupling inductor employed in a high performance ac power source," in Renewable Energy Research and Applications (ICRERA), 2012

International Conference on, Nov 2012, pp. 1–18.

[13] J. E. Huber and J. W. Kolar, "Analysis and design of fixed voltage transfer ratio dc/dc converter cells for phase-modular solid-state transformers," in 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Sept 2015, pp. 5021–5029.

[14] Y. K. Tran and D. Dujic, "A multiport medium voltage isolated dcdc converter," in IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Oct 2016, pp. 6983–6988.

[15] J. Huber, G. Ortiz, F. Krismer, N. Widmer, and J. W. Kolar, "η−ρ pareto optimization of bidirectional half-cycle discontinuous-conduction-mode series-resonant dc-dc converter with fixed voltage transfer ratio," in 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), March 2013, pp. 1413–1420.

[16] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "Zvs of power mosfets revisited," IEEE Transactions on Power Electronics, vol. 31, no. 12, pp. 8063–8067, Dec 2016.

[17] J. A. Anderson, L. Schrittwieser, M. Leibl, and J. W. Kolar, "Multi-level topology evaluation for ultra-efficient three-phase inverters," in 2017 IEEE International Telecommunications Energy Conference (INTELEC), Oct 2017, pp. 456–463.

[18] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-levelsystems,"IEEE Transactionson Industrial Electronics,vol.60, no. 12, pp. 5515–5527, Dec 2013.

[19] R. Erickson and D. Maksimovic, Fundamentals of Power Electronics. Springer US, 2001.

[20] M. Chen and J. Sun, "Feedforward current control of boost single-phase pfc converters," IEEE Transactions on Power Electronics, vol. 21, no. 2, pp. 338–345, March 2006.

[21] L. Harnefors, L. Zhang, and M. Bongiorno, "Frequency-domain passivity-based current controller design," IET Power Electronics, vol. 1, no. 4, pp. 455–465, December 2008.

[22] L. Harnefors, A. G. Yepes, A. Vidal, and J. Doval-Gandoy, "Passivitybased controller design of grid-connected vscs for prevention of electrical resonance instability," IEEE Transactions on Industrial Electronics, vol. 62, no. 2, pp. 702–710, Feb 2015.

[23] H. Bai, X. Wang, P. C. Loh, and F. Blaabjerg, "Passivity enhancement of grid-tied converters by series lc-filtered active damper," IEEE Transactions on Industrial Electronics, vol. 64, no. 1, pp. 369–379, Jan 2017.

[24] S.Busoand P.Mattavelli, Digital Control in Power Electronics. Morgan and Claypool Publishers, 2006.

[25] T. Nussbaumer, M. L. Heldwein, G. Gong, S. D. Round, and J. W. Kolar, "Comparison of prediction techniques to compensate time delays caused by digital control of a three-phase buck-type pwm rectifier system," IEEE Transactions on Industrial Electronics, vol. 55, no. 2, pp. 791– 799, Feb 2008.

[26] S. Bibian and H. Jin, "Time delay compensation of digital control for dc switch mode power supplies using prediction techniques," IEEE Transactions

on Power Electronics, vol. 15, no. 5, pp. 835–842, Sept 2000.

[27] P. R. Remus Teodorescu, Marco Liserre, Grid Converters for Photovoltaic and Wind Power Systems. Wiley-Blackwell, 2010.

[28] J. Lago and M. L. Heldwein, "Synchronous optimal pulsewidth modulation digital implementation concept for multilevel converters," in 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), March 2016, pp. 2833–2839.